PT-82

THIN-FILM INTRACORTICAL RECORDING MICROELECTRODES

Quarterly Report #5

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THIS QPR IS BEING SENT TO YOU BEFORE IT HAS BEEN REVIEWED BY THE STAFF OF THE NEURAL PROSTHESIS PROGRAM.

Thin-Film Intracortical Recording Microelectrodes

Summary

The goal of this contract is to develop a family of active recording probes suitable for fundamental studies in neurophysiology and for use in neural prostheses. The probes will have 64 sites, of which eight can be selected for use by the external world. The sites will be buffered on-chip. On one of the probes (PIA-2B/-3B), the neural signals will then be passed directly off chip, whereas on the other (PIA-2/-3) the signals will be amplified, multiplexed, and then passed off chip to minimize external leads. Both two-dimensional (2D) and three-dimensional (3D) configurations of these probes are being developed.

During the past term, we have continued to explore the chronic use of passive recording probes in-vivo. The most recent implant was removed after 100 days in-vivo and the tissue was examined. Tissue removal is now capable of showing fine details of the probe topography such as 3μm polysilicon surface features along the shanks. This helps in identifying the precise locations of the recording sites in tissue. Along most of the shank tracts, the tissue reaction was limited to a film of thickness less than 3μm. We have also continued to develop improved input dc stabiliization circuitry for eventual use with wireless versions of these probes. This circuitry is needed to avoid wasting a significant portion of the dynamic range at the input to the data converter that will be used prior to output transmission since the dc drift coming off the sites can be orders of magnitude larger than the neural signals. A promising approach using the conductance of a subthreshold MOS transistor has been explored and an improved recording amplifier is being designed.

The 64-site 8-channel 16-shank non-multiplexed recording probe PIA-2B/-3B is now being fabricated along with a 96-site 96-channel buffered probe. These devices are expected to be completed during the coming term. In the meantime, tests are continuing on the 2D and 3D active probes reported previously. During the past term, the external clock generation and demultiplexing circuitry for use with these probes was redesigned and acute neural recordings from active probes have been demonstrated for the first time using an external 5V clock and achieving high signal-to-noise ratios. This confirms that clocks can be suppressed to less than 10ppm using the probe structure. This is essential to the success of all future active recording probes and is a result that we have been seeking to establish for some time.

Thin-Film Intracortical Recording Microelectrodes

1. Introduction

The goal of this program is the realization of batch-fabricated recording electrode arrays capable of accurately sampling single-unit neural activity throughout of volume of cortical tissue on a chronic basis. Such arrays will constitute an important advance in instrumentation for the study of information processing in neural structures and should also be valuable for a number of next-generation closed-loop neural prostheses, where stimuli must be conditioned on the response of the physiological system.

The approach taken in this research involves the use of solid-state process technology to realize probes in which a precisely-etched silicon substrate supports an array of thin-film conductors insulated above and below by deposited dielectrics. Openings in the dielectrics, produced using photolithography, form recording sites which permit recording from single neurons on a highly-selective basis. The fabrication processes for both passive and active (containing signal processing circuitry) probe structures have been reported in the past along with scaling limits and the results of numerous acute experiments using passive probes in animals. In moving to chronic implant applications, the major problems are associated with the probe output leads, both in terms of their number and their encapsulation. The probe must float in the tissue with minimal tethering forces, limiting the number of leads to a few at most. The encapsulation of these leads must offer adequate protection for the megohm impedance levels of the sites while maintaining lead flexibility.

Our solution to this problem has involved two steps. The first has been to embed circuitry in the probe substrate to amplify and buffer the signals and to multiplex them onto a common output line. Using this approach, signal levels are increased by factors of about 300, impedance levels are reduced by four orders of magnitude, and the probe requires only three leads for operation, independent of the number of recording sites. A high-yield merged process permitting the integration of CMOS circuitry on the probe has been developed, and this circuitry has been designed and characterized. The second step has involved the development of silicon-based ribbon cables, realized using the same probe technology, to conduct the neural signals to the outside world. These cables have shown significant advantages over discrete leads, both in terms of the ease with which chronic implants can be assembled and in terms of the ability of the cables to survive long-term biased soaks in saline. The cables can be built directly into the probes so that they come off of the wafer as a single unit, requiring no joining or bonding operations between them. The cables are also significantly more flexible than previously-used discrete wire interconnects.

This contract calls for the development of active probes for neural recording. A 64-site 8-channel probe with site selection and signal buffering but no multiplexing is in development as is a high-end multiplexed version of this device that includes gain. During the past quarter, work concentrated in several areas: 1) we have continued efforts to explore chronic recording with platform-mounted "Brain-in-a-Box" passive probes, reaching 100 days with the latest implant; 2) we have successfully demonstrated multiplexed neural recording using an off-chip 5V clock with acceptable signal-to-noise ratios; 3) we have continued work to develop improved input circuitry for use with an integrated wireless version of the probe electronics; and 4) we have begun fabrication of the non-multiplexed 64-site 8-channel active recording probe. Work in these areas is discussed in the following sections.

2. *Passive Probe Developments*

In the last report, we described a chronic guinea pia auditory cortex implant which had been in place for 78 days. At that time, activity was present on 2 of the 12 possible channels of the brain-in-the-box array. The structure of this 3D probe assembly is reviewed in Fig. 1. Site rejuvenation (or biasing the site) had been successfully attempted on day 51. After day 78, biasing no longer increased the signal-to-noise of the sites and the animal was sacrificed on day 100 for post mortem analysis of the tissue.

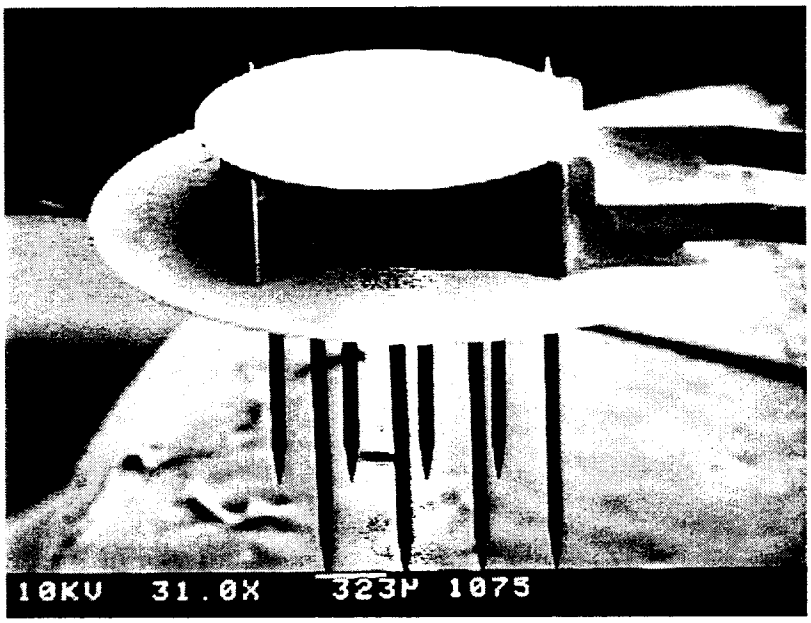

Fig. 1: The 3-D structure known as "Brain in the Box." The two cable strands which are integrated into the probes converge into a single main cable, resulting in the the two probes having sites which face one another. The shanks on this probe are spaced at 300μm.

The animal was heavily anesthetized and perfused through the heart with 4% paraformaldehyde in phosphate buffer. The brain was carefully dissected away from the cranium and the tissue was dissected to a small block containing the array. The array was removed and the tissue was embedded in JB4-glycol methacrylate resin. Five micron thick sections were cut perpendicular to the electrode tracts, stained with Paragon stain, and coverslipped with Permount mounting solution.

A photograph of one of the sections is shown in Fig. 2. Several interesting features can be noted from this section. First, a detailed cross-section of the electrode tract can be seen, indicating that this probe pulled out quite cleanly. One can actually observe three 3μm-wide polysilicon leads on this shank. This type of detail permits coding of the location of the tissue slice along the shanks. In this case, the slice is between the third and fourth sites from the tip. Polysilicon markers could be included on probe shanks to provide even more detailed information on location.

A second feature which can be noticed in the photograph is the presence of a "swirling" of the surrounding tissue on one edge of the shank (the top edge on Fig. 2). This type of morphology is typically seen at the shank tip and has been taken as an

indication of relative movement of the probe. In this case, the motion of the probe was in the direction of the interconnect, possibly indicating the presence of a tethering force.

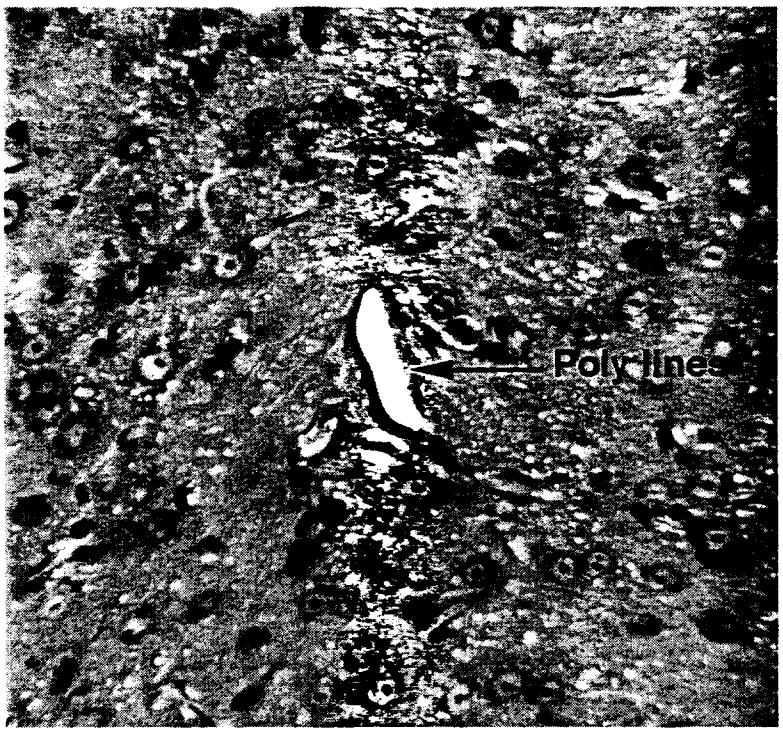

Fig. 2: Photomicrograph of the cross-section of a single shank tract from a brain-in-the-box array implanted in guinea pig auditory cortex for just over 3 months. The array was pulled out of the tissue prior to sectioning. The arrow points to two of the three imprints left from the polysilicon leads, which are only 3μm in width. The width of the probe shank was 60μm.

Finally, along most of the tracts, tissue reaction was limited to a film of thickness less than a polysilicon lead (3μm), indicating good acceptance of the implant by the tissue. Further analysis of this tissue will be performed in the coming weeks, and we will continue to implant and evaluate these arrays.

3. A Telemetry Interface for Multiplexed Recording Probes

We have begun developing the circuitry that will be needed to demonstrate a wireless chronic microprobe where both power and selection data is supplied via input telemetry and where neural data is relayed out in a similar fashion. Because data conversion will be performed on-chip prior to telemetry, it is important to achieve very low offsets and stable gains in the probe input circuitry so that the dynamic range of the data converter is not wasted. Thus, over the past quarter we have focused on developing a stable input amplifier with input offset suppresion. Over the last quarter we have accomplished the following goals in our research endeavors:

- Completion of the DC stabilization circuit design and validation of the circuit performance.
- Design, simulation and testing of a neural signal amplifier.
- Simulation of the entire system (i.e., the DC stabilization circuit along with the amplifier).

3.1 DC Stabilization Circuit Design

Figure 3 shows the block diagram of the new dc stabilization scheme that has been developed. Re, Ce, and Cp constitute the simplified electrode circuit model that was utilized for the simulations. The nominal values chosen for Re (electrode resistance), Ce (electrode-electrolyte capacitance) and Cp (parasitic capacitance) were 500GΩ, 150 pF, and 12 pF, respectively. Other components in the model, such as spreading resistance, interconnect resistance, etc., were neglected since these are much smaller in magnitude than the components illustrated in the above diagram.

Problem Of DC Stabilization:

DC stabilization of the input of the preamplifiers has been a continuing challenge and has still not been adequately resolved. It arises from the fact that the recorded neural signal is in the form of a small amplitude ac signal (typically of the order of 50 to 100μV) riding on a 100-200mV dc component. Such a large dc component, if allowed unchecked, would saturate the circuitry that follows the electrode.

A number of schemes have been developed to combat this problem, yet none of them have yielded a complete solution. These schemes include:

- Use of a diode or a diode clamp transistor to pin the dc potential to ground. This scheme suffers from susceptibility to optical effects and to leakage current variations.
- Use of a reset gate that sets the dc potential to zero during each recording frame. This circuit however suffers from injected noise problems.

Ideally, the dc potential could be clipped off with a single large resistance (above 40MΩ or so). However, it is next to impossible to fabricate such a large resistance in a standard CMOS process. Thus there is a need for a circuit solution that can yield a high resistance with a standard CMOS process and yet be free of optical and noise effects.

Solution To DC Stabilization Problem:

As mentioned in the previous Quarterly Report (Quarterly Report #4), we have developed a novel sub-threshold circuit solution for the problem of dc stabilization. Figure 3 shows transistor M which is driven by a voltage (Vgs in the figure) that is well below the threshold voltage of the device. Consequently, it offers a very high drain source resistance Rds (typically in the region of 25 to 75 MΩ). This is represented as "R" in the figure. It is clear that with the inclusion of R in the circuit, two effects come into play:

1. a high pass filtering action due to the combination of Ce and R
2. dc voltage division due to the combination of Re and R.

NON FEEDBACK DC STABILIZATION SCHEME

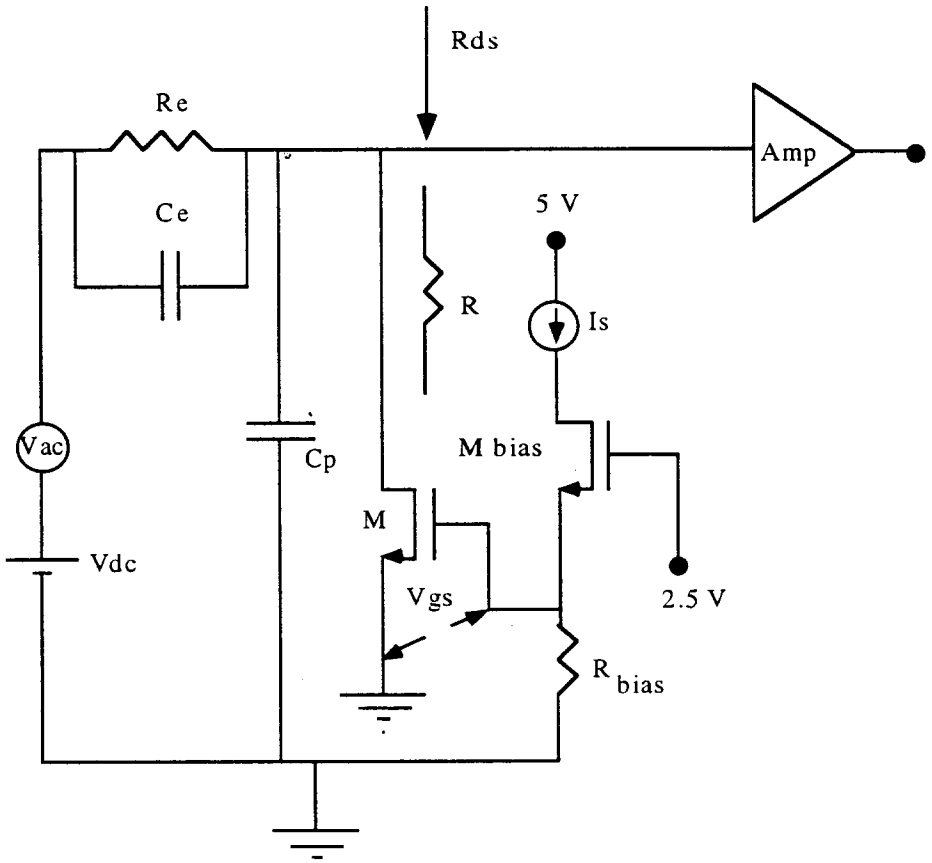

Fig. 3: Representation of the dc stabilization circuit explored during the past quarter.

Thus, if R is chosen in an optimal fashion, it is possible to nullify the dc component by means of resistive division, yet at the same time retain the ac component by ensuring that the high-pass cutoff frequency does not become too large (typically, it should not exceed 80 to 100 Hz). The reason subthreshold circuits have been chosen for this application is that only in the subthreshold region of operation can the device offer a resistance to the order of 50 to 80 MΩ or more.

From the above discussion, it is evident that the value of the gate-source voltage of the transistor M has to be carefully chosen so that it offers an optimum resistance. To accomplish this, a typical transistor was characterized in the subthreshold regime and its drain-source resistance was extracted from HSPICE simulations. Level 4 HSPICE was chosen for the simulations since it could adequately explain the behavior of the device at subthreshold. From the results of these simulations, the above circuit was developed. The biasing of the subthreshold transistor is accomplished by means of a source-degenerated transistor (M bias). The voltage across Rbias sets the gate source voltage of the transistor M. The "stabilized" signal is then amplified by a preamplifier "A". It is clear from the above figure that the operation of the circuit is critically dependent on the gate-source bias of M (which in turn depends on the resistance Rbias). The reason for this critical dependence is that in the subthreshold regime, the drain-source resistance falls off exponentially for a very small change in the gate bias and consequently the device must be

finely biased. It has been found that with the given HSPICE models a gate source voltage of 0.5 to 0.55V is necessary to ensure that the device offers a subthreshold resistance of around 75MΩ.

Performance Of The Circuit:

Figure 4 shows the ac and the transient performance of the above circuit at 27°C. The top panel shows a typical representation of the recorded signal, i.e. a small amplitude ac signal riding on a varying dc component. In order to test robustness of the circuit, the dc variation was chosen to be quite fast. The middle panel shows the stabilized signal. This is the recovered sinusoid with negligible attenuation. One can clearly see that the dc component has been removed. Figure 5 shows the Bode plot of the system as well as the input referred noise voltage magnitude (integrated over the bandwidth of 5Hz to 15kHz). This panel indicates that the high pass cut off frequency is around 50Hz and is thus below the useful signal bandwidth.

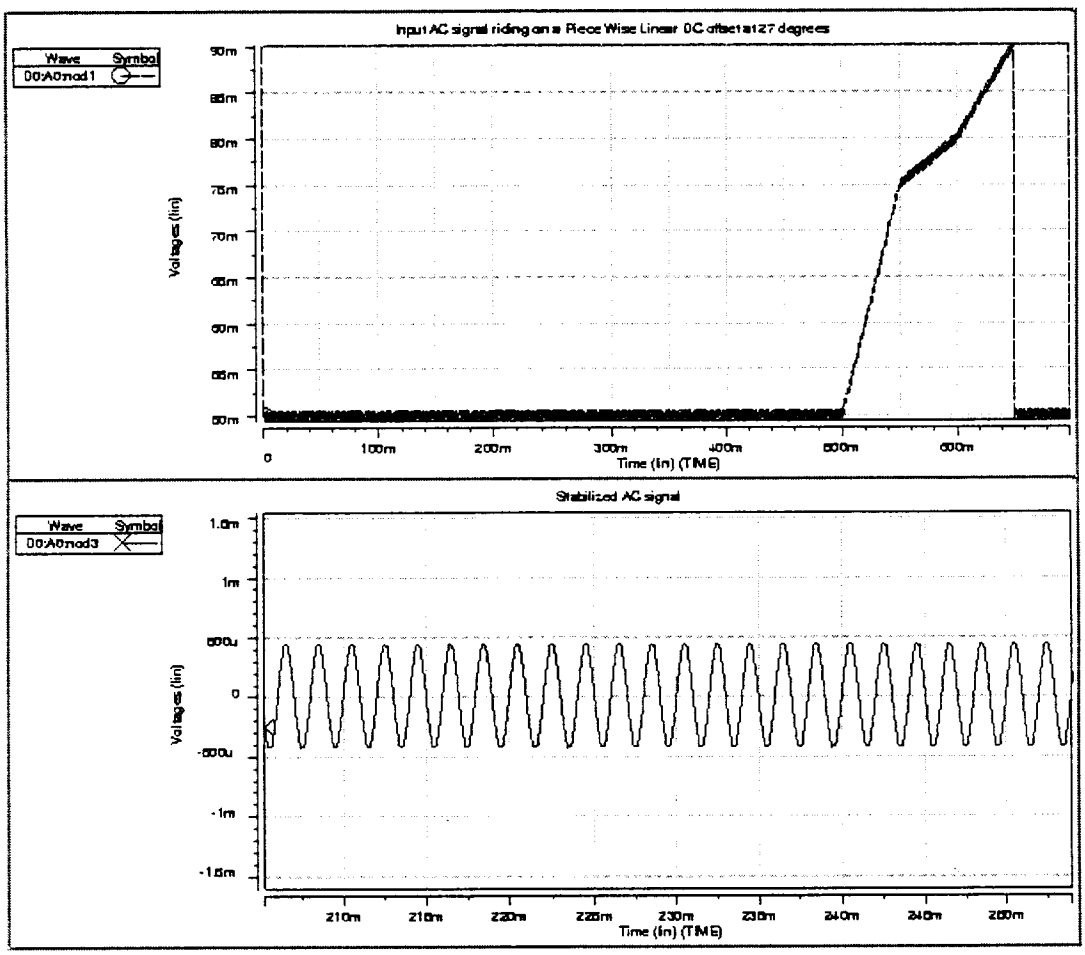

Fig. 4: Transient response of the input stabilization circuit at 27°C.

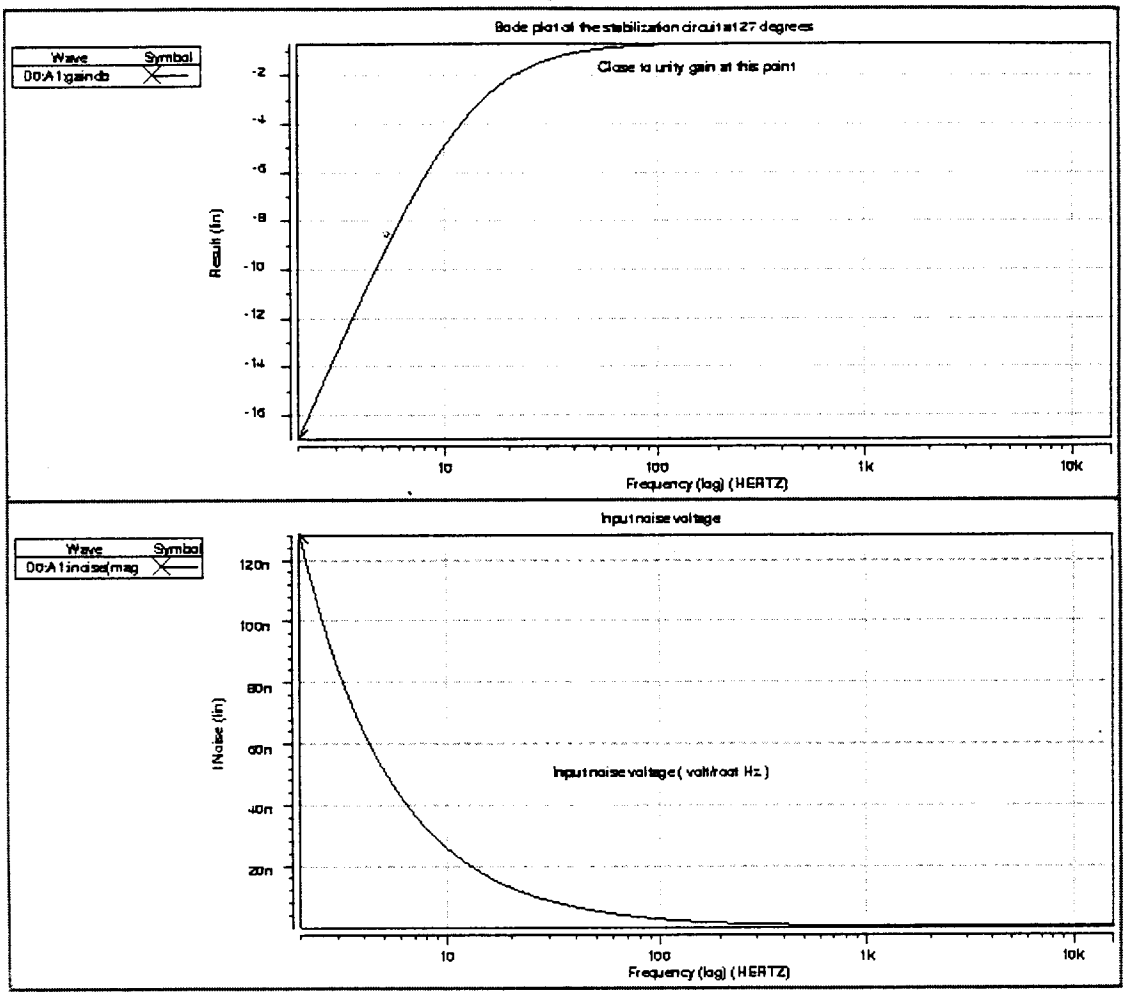

Fig. 5: Bode plot and input noise voltage magnitude of the stabilized input circuit at 27°C.

A number of such simulations were carried out in order to test the robustness of the circuit. These simulations included

1. Testing against temperature variations. The circuit simulations were done at 2 temperatures, 27 and 37°C (body temperature). The results of these simulations are shown below as Figs. 6 and 7. They are also summarized below as

PARAMETER TESTED	*27 DEG. CELSIUS*	*37 DEG. CELSIUS*
Input signal	20 μV	20 μV
Stabilized signal	18.5 μV (>100 Hz)	18.5 μV (>100 Hz)
Input referred noise voltage (integrated from 0-15 kHz)	50 to 70 nV/root Hz	50 to 70 nV/root Hz
Process stability	±10%	±10%

2. *Testing against process variations.* The fabrication process may not deliver the parameters that were used for the simulations and so the circuit was tested for robustness to process variations. It was found that the circuit was stable to process variations (in the threshold voltages) up to 10-15 % in either direction. It was extremely robust with respect to changes in other process parameters. It is believed that process parameter variations will be well below 10%.

3. *Testing against noise effects.* The circuit has a very low equivalent input noise signal magnitude. The high pass filter (formed by Ce and R) shapes the noise signal and restricts it to between 50 to 70 nV/root Hz, integrated over a bandwidth from 0 to 15 kHz (for a 20μV ac input).

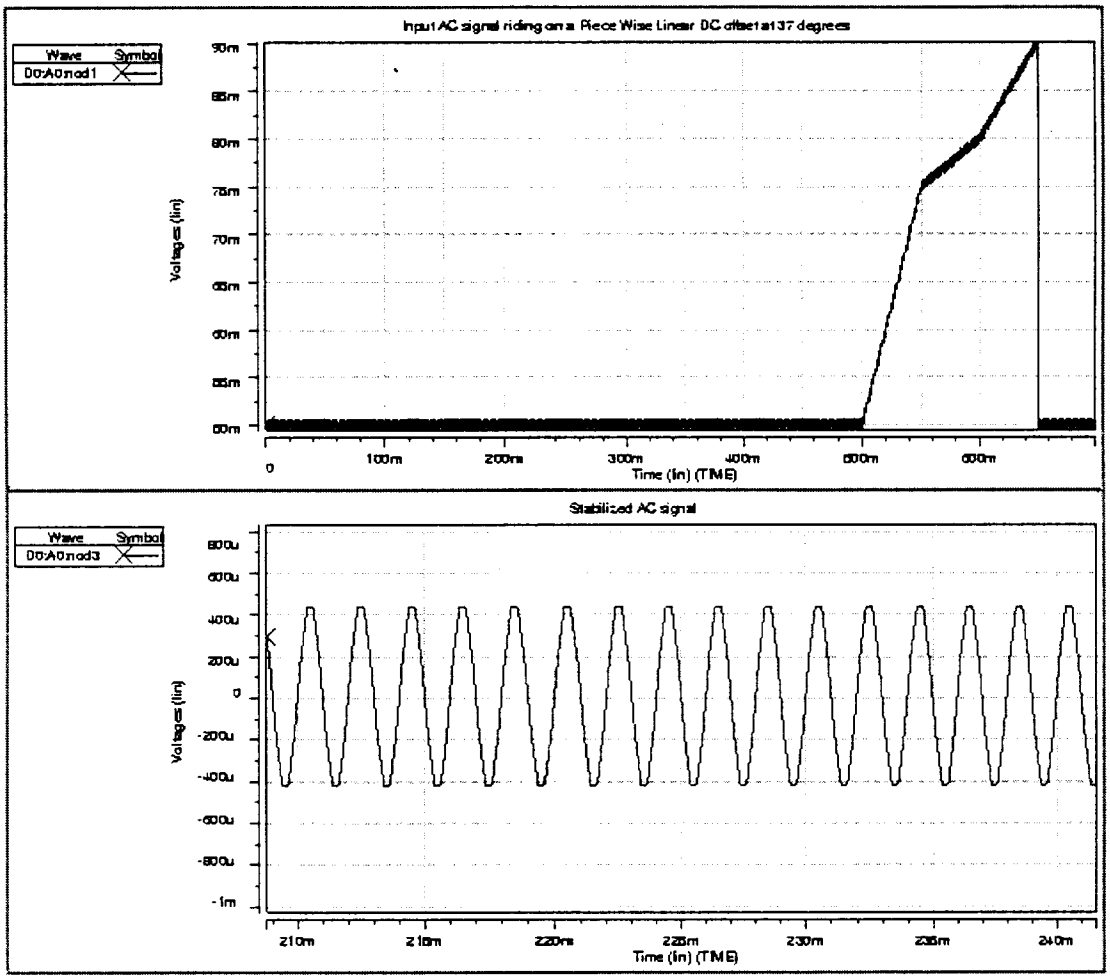

Fig. 6: Transient response of the input circuit at 37°C.

In conclusion, a promising open-loop subthreshold circuit solution for DC stabilization has been developed that consumes low power, has a very low noise voltage, and is relatively free from optical effects. The circuit has been simulated extensively and been found to be quite robust.

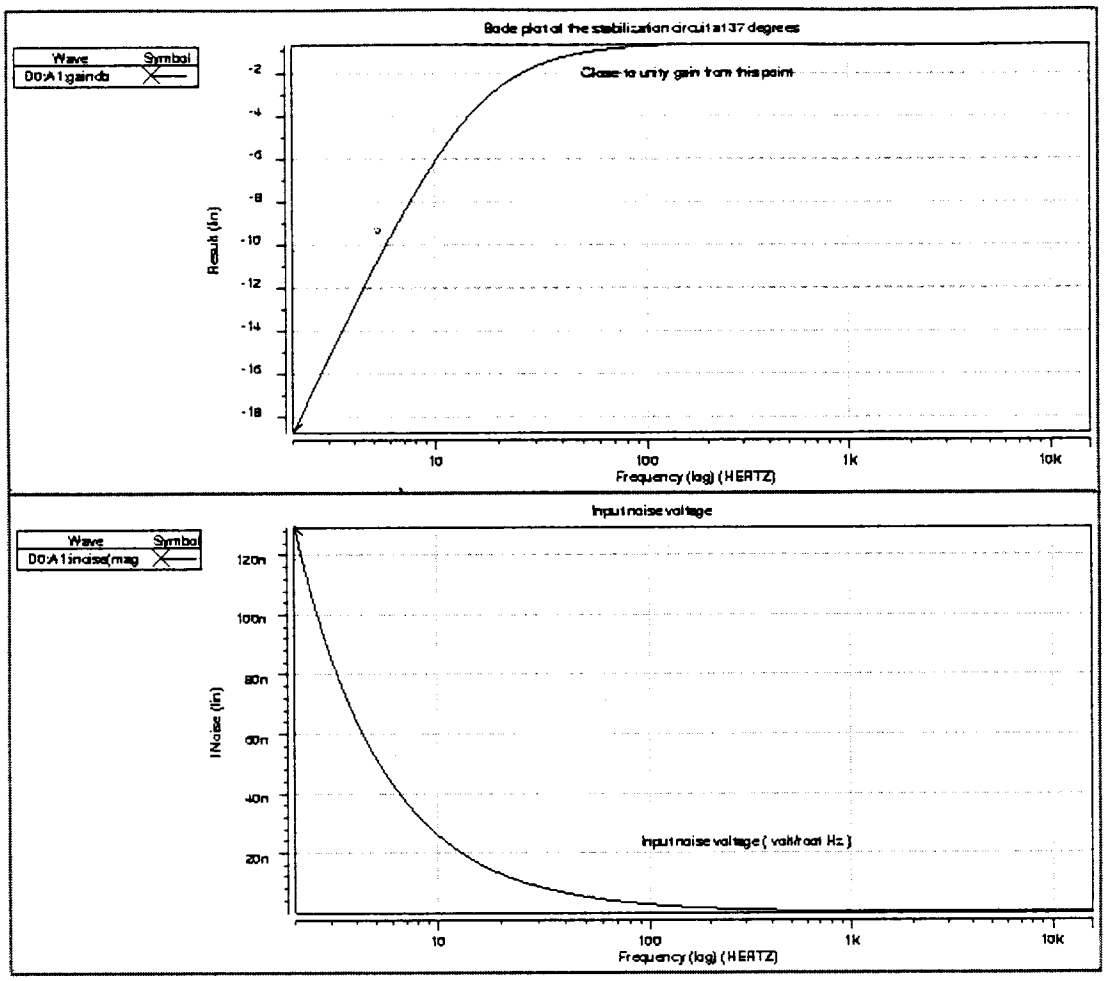

Fig. 7: Bode plot and input noise voltage magnitude at 37°C.

3.2 Design of the Input Amplifier

Over the last quarter ,we have also designed and simulated a neural signal amplifier. This was done with a view to completing the system that is associated with the dc stabilization stage outlined in Fig. 3.

A variety of amplifiers for neural signal applications have been developed at Michigan. The most successful one was an open loop amplifier that employed dc feedback to decrease the gain at low frequencies (thus ensuring that the resultant gain at frequencies above 100 Hz was the ac open-loop gain of the amplifier). However, although this amplifier did prove to be reasonably successful, it has been observed that the gain is dependent on process parameters such as gate oxide thickness and threshold voltage. The main reason behind this drawback was that the amplifier was not closed-loop and therefore displayed variable gain. To overcome some of these shortcomings, we have been studying the design of a new amplifier circuit that can provide the following overall features:

1. moderate to high gain (30 to 50 dB).
2. low frequency feedback to reduce the dc gain of the circuit.
3. incorporation of closed-loop feedback in order to stabilize the gain.

4. constant passband gain across wafer/devices
5. reduced noise voltage contributed by the amplifier.
6. high input voltage range.
7. high CMRR and phase margin

Our initial approach towards satisfying some of these requirements is shown in the block diagram in Fig. 8. It can be seen that we plan to have dual feedback loops. One of the loops is to reduce the gain at low frequencies and the other serves the purpose of stabilizing the gain.

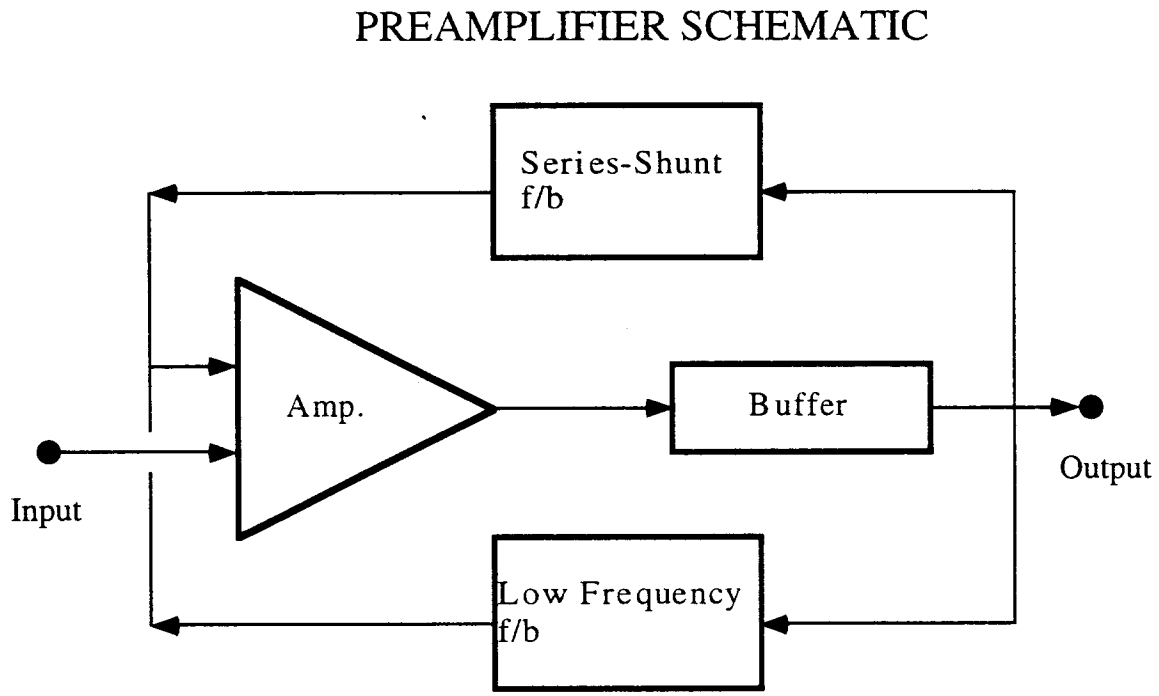

Fig. 8: Block diagram of the proposed input amplifier.

We are planning on using MOS transistors operated in the linear region as feedback elements; however, it is not yet clear whether this can be done reliably and at low voltages. A preliminary design has been performed, and simulations have also been done on this amplifier as well as upon an integrated system consisting of the dc stabilization stage along with the preamplifier and promising results have been obtained. Work is still being carried out towards optimizing the preamplifier performance (mainly by reducing power consumption and increasing gain). The results of this design and a more detailed discussion of the amplifier circuit will be presented in the next progress report.

In the coming quarter, we plan to complete the preamplifier design and integrate it with the dc stabilization unit in order to obtain a complete system.

4. *Development of a 64-Site Eight-Channel Non-Multiplexed Recording Probe (PIA-2B)*

In the last quarterly report, the design of a 64-site buffered and front-end selected recording probe was presented. This probe represents the state-of-the-art in active neural probe design at the University of Michigan. The majority of the circuit blocks on the probe have previously been fabricated and tested on other probes, and the fabrication process has now been used on several recent successful active probe runs. The probe has been designed in both 2D and 3D versions, with both 8 and 16 shanks per probe. There are several test modes which have previously been described, and it is possible to pass current to the sites for activation or conditioning. The output signals are buffered with source followers having output impedances on the order of 10-20 kohms.

The masks for PIA-2B have been made, and fabrication of the probe has begun. The p-wells have been implanted and driven in, and deep and shallow boron diffusions have been carried out to define probe areas and tips. Deposition of the lower dielectrics and definition of the circuit area is currently underway. The most serious threat to device yield, the boron diffusions, have been accomplished without a significant loss of wafers. We expect these probes to be completed during the coming quarter.

5. *A 96-Site Buffered Recording Probe*

A 96-site buffered probe utilizing the same source followers used on PIA-2B was designed and included on the above mask set. The probe has six shanks with sixteen sites per shank and is being developed for Dr. Gyorgy Buzsaki at Rutgers. The output pads are spaced on 150μm centers, allowing for connection to a preamplifier board through a commercially available flex cable. This probe will be useful for researchers currently recording from a large number of sites who wish to improve the signal to noise ratio over that typical of a passive probe. It should also allow an opportunity to evaluate the performance of the output buffers on active recording probes.

Figure 9 is a semilog plot of the simulated output impedance from the buffers versus power dissipation for a range of supply voltages between 3 and 5V. The curve has a characteristic L shape, suggesting that by reducing the supply from 5 to 3.5V, significant decreases in power dissipation can be achieved without a large increase in output impedance. Below 3.5V, the curve slopes sharply upwards, indicating an increase in output impedance with little further decrease in power dissipation. At a supply voltage of 3.5V, the power dissipation of one buffer is approximately 20μW, for a total probe dissipation of 2mW. This is more than an order of magnitude lower than the power dissipation expected at 5V.

Since the probe contains only the buffers, there is no digital circuitry which would be affected by changing the supply voltage. By looking at active recordings at various supply voltages, and comparing them to recordings with the buffers switched out, we will be able to gain useful information about the effect of output impedance on signal to noise ratio. The probe is designed with the buffers at the very periphery of a large probe body which will protrude from the tissue in an acute preparation. Since the penetrating shanks are physically continuous with the probe body, and silicon is a fairly good conductor of heat, it remains to be seen how much heat will be conducted down through the shanks into the tissue. It is hoped that by adjusting the supply voltage we will be able to find a suitable tradeoff between output impedance and power dissipation, and certainly at dissipation

levels below 10mW for the overall probe, no significant heating of the embedded probe is expected.

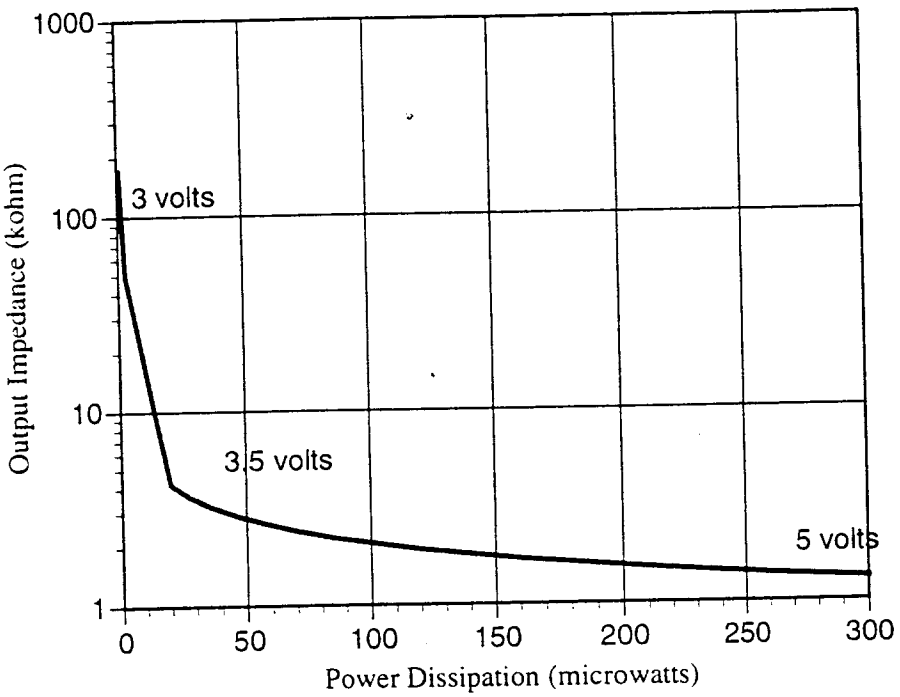

Fig. 9: Output impedance versus power dissipation for the source follower used on PIA-2B. The supply voltage increases from 3V to 5V from left to right along the curve.

6. *Active Three-Dimensional Recording Probe Arrays*

In order to instrument a large population of neurons simultaneously and to achieve high-quality neural recordings, advanced microelectrode arrays with on-chip signal processing circuitry are critically needed. Such active probes would lower the output impedance of the recording channels, improve the signal-to-noise ratio, reduce the number of the interconnection leads, and ease the encapsulation requirement of the recording systems. Several important accomplishments have been made recently in the area of process development. The process now consistently yields a low contact resistance on all sorts of contacts such as circuit contacts, recording sites and bonding pads. There are improvements on the LTO coverage over the circuit metal and the adhesion of gold lead transfers on the 3D arrays. The passivation of probe interconnects is further enhanced to minimize signal attenuation and noise coupling. A technique has also been developed to ensure that the active probes are released properly in EDP without having their circuit area being undercut. This technique is based on deep-etched slots around the shanks and wings of active probes so that these area are released solely by the front-side silicon etch, leaving thick silicon under the circuit areas. Using dielectric bridges for corner compensation at the outer corners of the circuit areas is also important in protecting these areas from what would otherwise be very rapid EDP undercutting. The full active probe process has now been run successfully with high yield. The resulting active probes are being tested in-vitro and in-vivo. Active 3D arrays have also been created by microassembling finished 2D active probes.

A set of active recording probes have been designed and fabricated recently in which each probe design tests a certain basic circuit function, including buffering, amplification, and multiplexing. The evaluations of these circuit blocks in terms of power, area, noise, and gain, and the detailed study of issues such as dc baseline stability, multiplexer clock noise, and the role of the bias applied to the probe substrate, is setting the stage for the circuit blocks to be used in higher-level probes (PIA-2B above and PIA-2, to be iterated later this year). As reported previously, we have been testing these active probes extensively and have presented successful in-vivo recordings using some of the probe designs in past reports.

We have designed and tested three different types of buffered probes, namely "BUF1", "BUF2", and "BUF3". The probe "BUF1" uses a simple source follower to buffer the signal output. It is a robust design (less sensitive to CMOS threshold shift), typically having a gain between 0.8 and 0.9 and using small area but relatively high power. The buffer in the probe "BUF3" is a complicated non-inverting unity-gain operational amplifier. It has very low output impedance, a high power supply rejection ratio, and consumes less power. Its only drawback is relatively large layout area. The complexity of the third buffer configuration "BUF2" is between the first two designs. This buffer is a two-stage push-pull type whose efficiency is four times of what the "BUF1" has, which means that it consumes less power as well as less area. But because of its two stages, the gain of "BUF2" is only around 0.7. We have demonstrated that all three buffered probes are capable of recording high-quality single-unit neural activity. And by comparing data obtained simultaneously from the same cell by passive (non-buffered) and active (buffered) recording electrodes only 15μm apart, we have concluded that on-chip signal processing is possible without compromising signal-to-noise ratios.

We previously reported in-vivo neural recordings using our multiplexed probe "MUX1". This probe contains four front-end buffers and a 4:1 multiplexer using off-chip clock. It is the first time that isolated neurons have been recorded through multiplexed signal channels on-chip and then demultiplexed off-chip. It is also the first time that we have used an off-chip clock with such a multiplexer. However, significant noise feedthrough was observed during those experiments, including one low-frequency noise component at about 180Hz. During the past quarter, we have worked to identify the noise sources and improve the signal-to-noise level. As detailed below, we have reduced the noise feedthrough of the external demultiplexing system significantly by building a new clock generator for the on-chip multiplexer and the external demultiplexer and by replacing the second-stage amplifier of the demultiplexing system with a lower-noise one. By using the improved system, we have recorded single-unit neural activity of better quality with the probes "MUX1" and "MUX3".

As there is more and more demand for multi-site recording microelectrodes and large 3D probe arrays, it is of great interest to develop active probes so that external lead counts can be reduced by multiplexing the recording channels and/or selecting sites close to active neurons. For an active 3D probe, an external clock is necessary because it is required for clock synchronization among the multiple probes of the array. The use of off-chip clock also has the advantage of simplifying the on-chip circuitry and the external demultiplexing system. However, the potential noise problems associated with the multiplexed probes, such as switching noise, clock coupling, and aliasing, pose quite a challenge to the design of active multiplexed probes and their external demultiplexing system. To overcome these noise problems, care has been taken in both circuit design and layout. For example, the signal channel has low output resistance to minimize clock coupling. CMOS analog switch is used to reduce switching noise feedthrough. Also, separate n-pockets are used for analog and digital circuitry to prevent noise feedthrough during clock transition.

Among the four designs of the multiplexed probes, the probe "MUX1" is the simplest. Its four signal channels are each buffered by a source follower (the same as that in the probe "BUF1") and are then multiplexed into one output channel. The multiplexer consists of a 4-bit counter made of static d-type flip-flops and 4 pairs of CMOS switches. The schematic of the overall mux-demux system is shown in Fig. 10. As reported previously, we have been able to record signal-unit neuron responses using the probes "MUX1". But the noise level of the recorded signals was significant. The subsequent in-vitro experiments have indicated that part of the noise resulted from the earth ground. The earth ground was used in those recording experiments because the off-chip clock was generated by a commercial function generator. To avoid this kind of noise feedthrough, a clock generator has been built using off-shelf IC chips. It is powered by batteries so that it can be completely isolated from the earth ground. We have also found that the second-stage amplifiers (the operational amplifier in MF6-50) are quite noisy, so we used our 16-channel amplifier system instead.

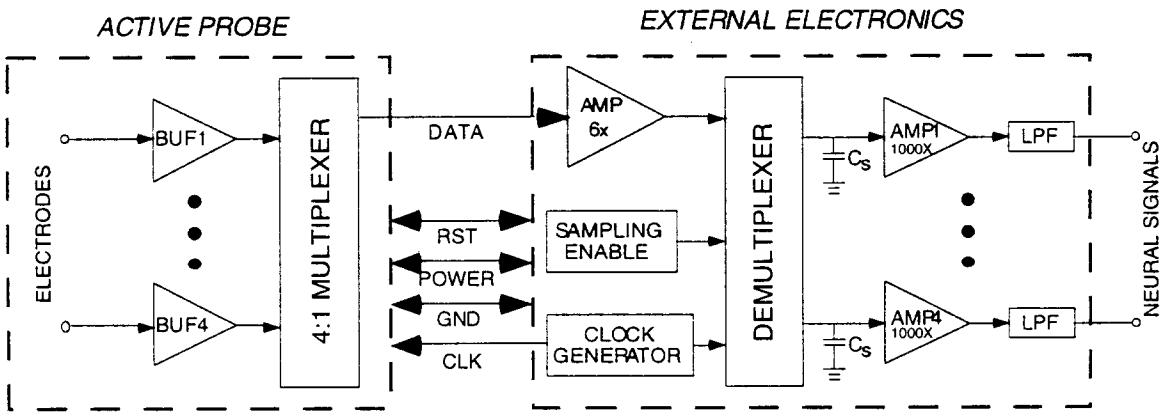

Fig. 10: System diagram of the probe "MUX1" and its external demultiplexing electronics.

As shown in Figs. 11 and 12, we have obtained much better neural recordings with the probes "MUX1" by using the improved external system. The signal-unit neuron activity shown in Fig. 11 was recorded in guinea cochlear nucleus, driven by white noise bursts. The first two channels do not show any neural responses simply because the corresponding electrodes were not inserted into the tissue at that time. But they do reflect the background noise level. On the other hand, significant neural activity was recorded with good signal-to-noise ratios by channels 3 and 4, especially channel 3. Figure 12 shows the spontaneous neural responses recorded by the probe "MUX1".

We have also recorded neural signals using another kind of multiplexed probe, "MUX3". This probe is very similar to the probe "MUX1" except its buffer is a unity-gain op amp, the same as that in the probe "BUF3". Although we were expecting the noise performance of "MUX3" to be better that of "MUX1" because of its higher PSRR (power supply rejection ratio), the recorded signals shown in Figures 3 and 4 actually have larger noise levels. We believe this is partially due to the fact that the clock used by "MUX3" is noisier than that of "MUX1". The two clocks were generated somewhat differently since "MUX3" needs ±2.5V clock while "MUX1" uses +5V clock. We are going to rebuild and improve the clock generator for "MUX3" and explore this issue further.

To investigate the noise levels generated at each stage of the mux-demux system, we have conducted a series of in-vitro experiments with the probe "MUX1". In the

frequency range of 300Hz to 3kHz, the average noise level of the external demultiplexing system is about 3μV-rms. This noise can be reduced further by increasing the gain of the first-stage amplifier shown in Fig. 10 and by optimizing the sampling and delay windows of the demultiplexer. With the on-chip multiplexer disabled (the clock was running but the counter was reset all the time; this means only channel 1 was selected), the noise level of the buffering and demultiplexing system is less than 9μV-rms. The thermal noise at the electrode-electrolyte interface attributes most of the noise (~7μV-rms --- this number includes the noise of the external amplifying stages). This implies that clock coupling through the output leads is insignificant in this case. When the mux-demux system runs fully, the overall noise is less than 14.5μV-rms. This additional noise is results from the switching and multiplexing on-chip. Several methods may be used to reduce the above multiplexing noise, including better design and layout, providing a clean clock signal, and increasing the output drive capability. But the most effective way to minimize such noise is probably to provide a gain-stage and band limiting before the multiplexing. In fact, two multiplexed probes with preamplifiers have been designed. However, due to the dc-offset problem, we have not yet used these two probe designs in recording experiments. Experiments with these probes will take place once we resolve the problem.

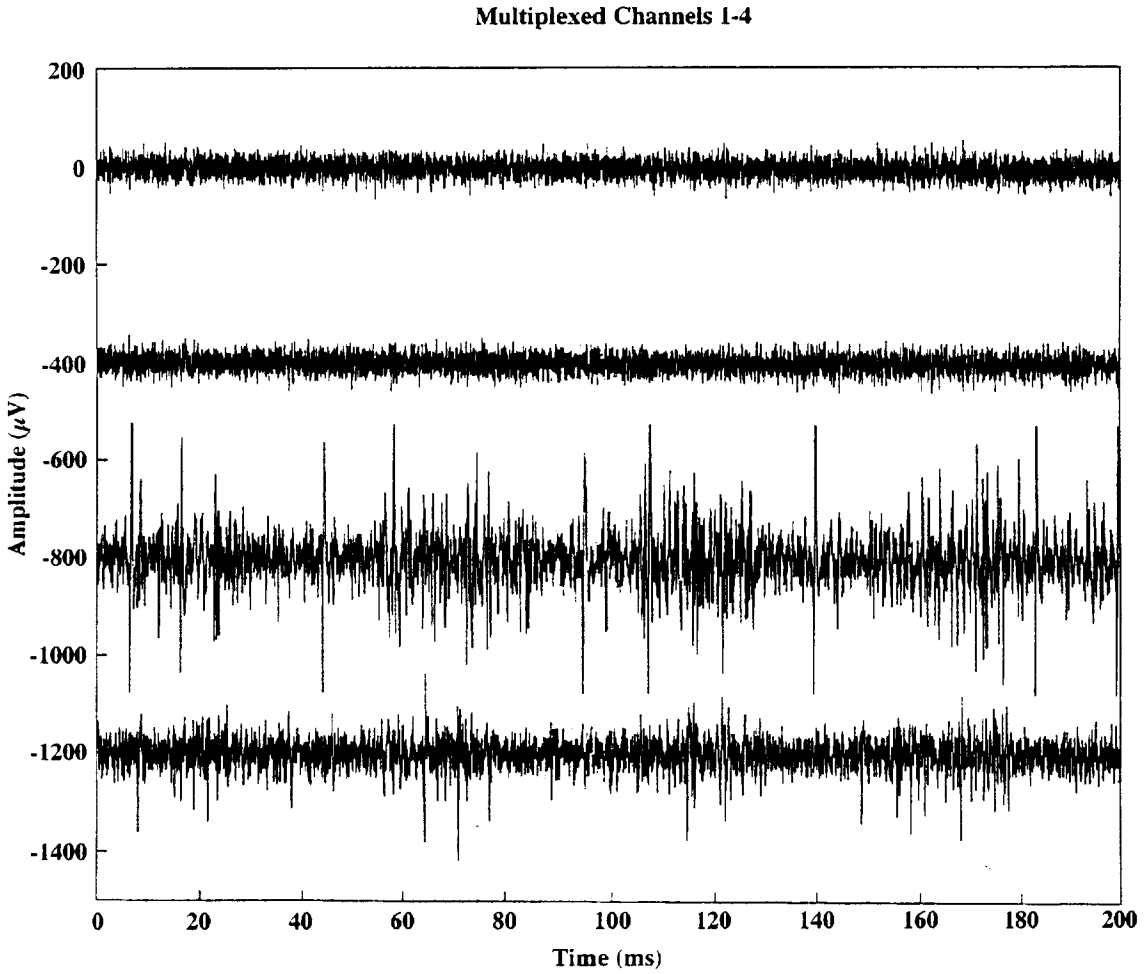

Fig. 11: Single-unit neural responses driven by white noise burst recorded with probe "MUX1" in guinea pig cochlear nucleus.

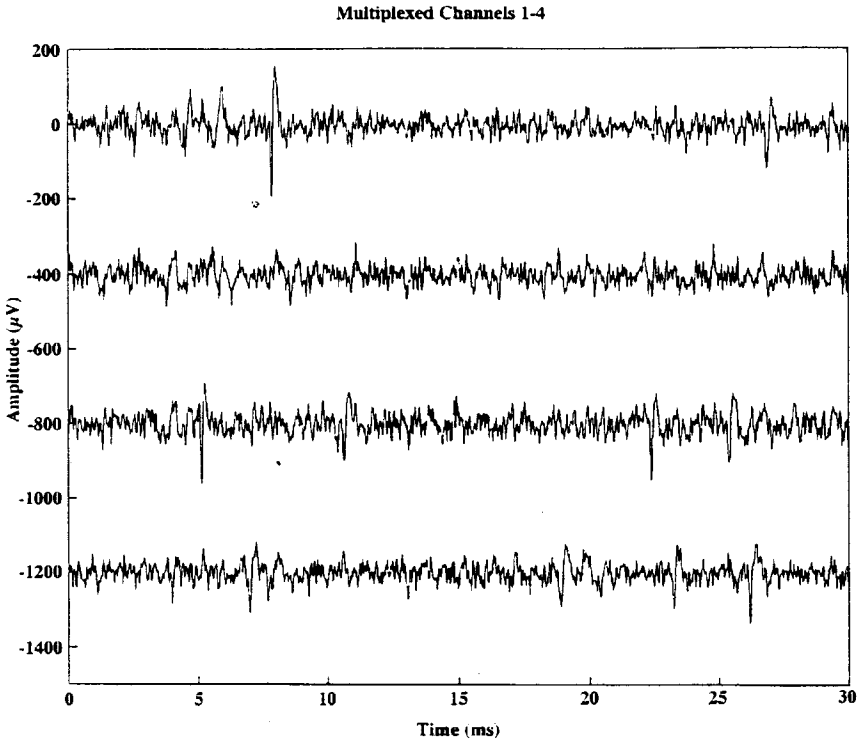

Fig. 12: Spontaneous neuron activity recorded with probe "MUX1" in guinea pig cochlear nucleus.

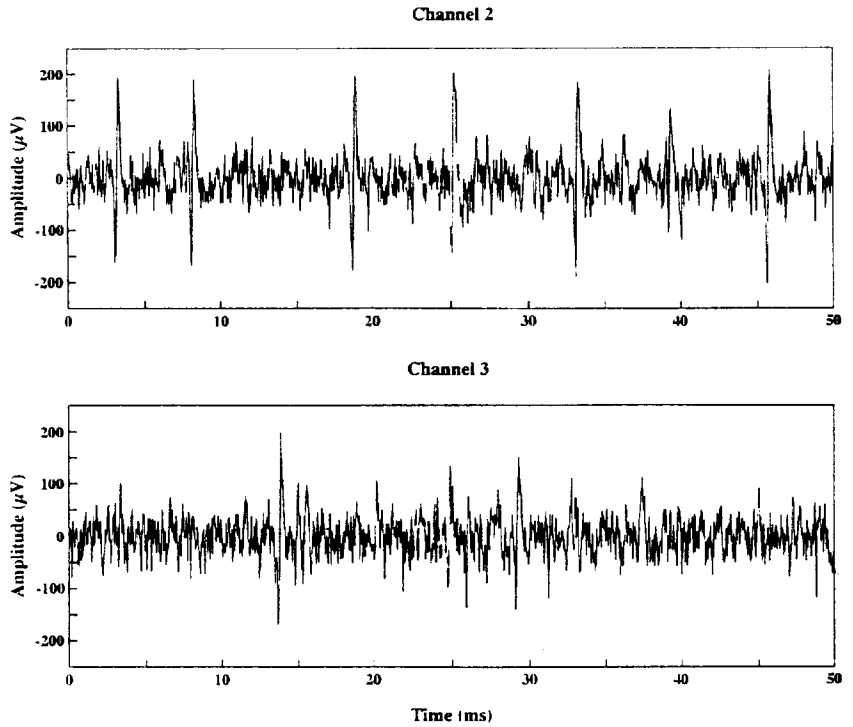

Fig. 13: Single-unit noise-driven responses recorded with the probe "MUX3" in guinea pig cochlear nucleus.

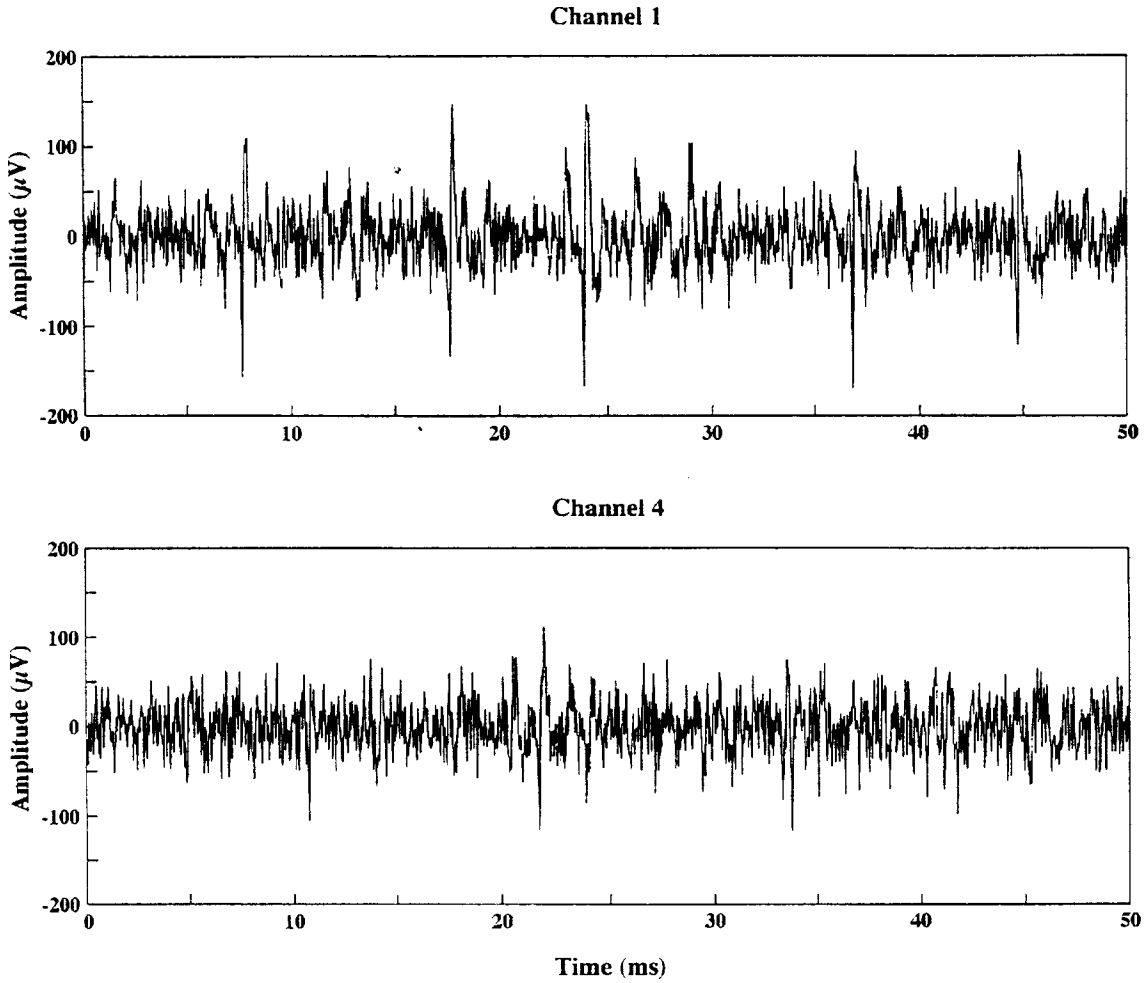

Fig. 14: Spontaneous neuron signals recorded with probe "MUX3" in guinea pig cochlear nucleus.

7. *Conclusions*

The goal of this contract is to develop a family of active recording probes suitable for fundamental studies in neurophysiology and for use in neural prostheses. The probes will have 64 sites, of which eight can be selected for use by the external world. The sites will be buffered on-chip. On one of the probes (PIA-2B/-3B), the neural signals will then be passed directly off chip, whereas on the other (PIA-2/-3) the signals will be amplified, multiplexed, and then passed off chip to minimize external leads. Both two-dimensional (2D) and three-dimensional (3D) configurations of these probes are being developed.

During the past term, we have continued to explore the chronic use of passive recording probes in-vivo. The most recent implant was removed after 100 days in-vivo and the tissue was examined. Tissue removal is now capable of showing fine details of the probe topography such as 3μm polysilicon surface features along the shanks. This helps in identifying the precise locations of the recording sites in tissue. Along most of the shank

tracts, the tissue reaction was limited to a film of thickness less than 3μm. We have also continued to develop improved input dc stabiliization circuitry for eventual use with wireless versions of these probes. This circuitry is needed to avoid wasting a significant portion of the dynamic range at the input to the data converter that will be used prior to output transmission since the dc drift coming off the sites can be orders of magnitude larger than the neural signals. A promising approach using the conductance of a subthreshold MOS transistor has been explored and an improved recording amplifier is being designed.

The 64-site 8-channel 16-shank non-multiplexed recording probe PIA-2B/-3B is now being fabricated along with a 96-site 96-channel buffered probe. These devices are expected to be completed during the coming term. In the meantime, tests are continuing on the 2D and 3D active probes reported previously. During the past term, the external clock generation and demultiplexing circuitry for use with these probes was redesigned and acute neural recordings from active probes have been demonstrated for the first time using an external 5V clock and achieving high signal-to-noise ratios. This confirms that clocks can be suppressed to less than 10ppm using the probe structure. This is essential to the success of all future active recording probes and is a result that we have been seeking to establish for some time.